AMENDMENTS TO THE CLAIMS

Claims 1-4 (cancel):

Claim 5 (currently amended): A method ~~as in claim 1~~ for writing to a memory element, said method comprising:

precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor; and

coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element;

wherein said associated capacitance comprises a capacitor coupled to said conductor.

Claim 6 (currently amended): A method ~~as in claim 1~~ for writing to a memory element, said method comprising:

precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor; and

coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element;

wherein said associated capacitance comprises a parasitic capacitance of said conductor and a capacitor coupled to said conductor.

Claim 7 (cancel):

Claim 8 (currently amended): A method ~~as in claim 2~~ <u>for writing to a memory element, said method comprising:</u>

<u>precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor; and</u>

<u>coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element;</u>

wherein said first voltage is at or approximately <u>a supply voltage</u> ~~at Vdd~~ and said second voltage is <u>approximately one half of said supply voltage.</u> ~~Vdd/2.~~

Claim 9 (currently amended): A method ~~as in claim 3~~ <u>for writing to a memory element, said method comprising:</u>

<u>precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor; and</u>

coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element;

wherein said first voltage is ground and said second voltage is at or approximately at one half of a supply voltage. ~~Vdd/2.~~

Claims 10-11 (cancel):

Claim 12 (currently amended): A method ~~as in claim 11~~ for writing to a memory element, said method comprising:

precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor; and

coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element;

wherein said memory element comprises a chalcogenide glass memory element and said chalcogenide glass memory element comprises a germanium:selenium glass composition which is doped with silver.

Claims 13-16 (cancel):

Claim 17 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element;

wherein said first predetermined voltage is at or approximately at one half of a supply voltage ~~Vdd/2~~ and said second predetermined voltage is at or approximately at said supply voltage. ~~Vdd.~~

Claim 18 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element;

wherein said first predetermined voltage is at or approximately at one half of a supply voltage ~~Vdd/2~~ and said second predetermined voltage is at or approximately at ground.

Claim 19 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element;

wherein said act of applying a first predetermined voltage comprises coupling a cell plate, to which said first terminal is coupled, to a source of said first predetermined voltage.

Claim 20 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element; and

selectively coupling at least one capacitor to said bit line to store said second predetermined voltage.

Claim 21 (original): The method of claim 20 further comprising enabling a transistor to selectively couple at least one capacitor to said bit line.

Claim 22 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element;

wherein said parasitic capacitance has a value of about 500 fF.

Claim 23 (currently amended): A ~~The~~ method ~~of claim 13~~ for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element; and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element;

wherein said programmable conductor memory element comprises a chalcogenide glass.

Claim 24 (original): The method of claim 23 wherein said chalcogenide glass comprises a Ge:Se glass composition which is doped with silver.

Claims 25-28 (cancel):

Claim 29 (currently amended): A ~~The~~ method of ~~claim 25~~ operating a memory cell ~~further~~ comprising:

precharging a bit line to a first voltage;

applying a second voltage to a first terminal of a chalcogenide memory element;

connecting a second terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element; and

selectively coupling at least one capacitor to said bit line to receive and store said first voltage.

Claim 30 (original): The method of claim 29 further comprising operating a transistor to selectively couple said at least one capacitor to said bit line.

Claim 31 (currently amended): A ~~The~~ method of ~~claim 25~~ operating a memory cell comprising:

precharging a bit line to a first voltage;

applying a second voltage to a first terminal of a chalcogenide memory element; and

connecting a second terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element;

wherein said bit line has a parasitic capacitance of about 500 fF.

Claim 32 A ~~The~~ method of ~~claim 25~~ operating a memory cell comprising:

precharging a bit line to a first voltage;

applying a second voltage to a first terminal of a chalcogenide memory element; and

connecting a second terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element;

wherein said chalcogenide memory element comprises a Ge:Se glass composition doped with silver.

Claims 33-34 (cancel):

Claim 35 (cancel): A memory structure comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

Claim 36-37 (cancel):

Claim 38 (currently amended): A ~~The~~ memory structure ~~of claim 37~~ comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said precharge circuit supplies a first voltage of a supply voltage to program a higher resistance state into said memory element and a second voltage of ground potential as said first voltage to program a lower resistance state into said memory

element, ~~said first value is at or approximately at Vdd, said second value is ground,~~ and said second voltage is at or approximately at one half of said supply voltage. ~~Vdd/2.~~

Claim 39 (cancel):

Claim 40 (currently amended): A ~~The~~ memory structure ~~of claim 35~~ comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 41 (currently amended): A ~~The~~ memory structure ~~of claim 35~~ comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claims 42-43 (cancel):

Claim 44 (currently amended): A ~~The~~ memory structure ~~of claim 43~~ comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said memory element comprises a chalcogenide glass memory element and said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

Claims 45-47 (cancel):

Claim 48 (currently amended): A ~~The~~ semiconductor memory ~~of claim 45~~ comprising:

a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;

a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;

a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and

an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line;

wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 49 (currently amended): A ~~The~~ semiconductor memory ~~of claim 45~~ comprising:

a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;

a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;

a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and

an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line;

wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claim 50 (original): The semiconductor memory of claim 48 further comprising a switching device for selectively coupling said at least one capacitor to said bit line.

Claim 51 (original): The semiconductor memory of claim 49 comprising a switching device for selectively coupling said at least one capacitor to said bit line.

Claim 52 (cancel):

Claim 53 (currently amended): A ~~The~~ semiconductor memory ~~of claim 52~~ comprising:

a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;

a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;

a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and

an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line;

wherein said memory element comprises a chalcogenide glass memory element and said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

Claim 54 (currently amended): A ~~The~~ semiconductor memory ~~of claim 47~~ comprising:

a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;

a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;

a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and

an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line;

wherein said parasitic capacitance has a value of about 500 fF.

Claims 55-57 (cancel):

Claim 58 (currently amended): A ~~The~~ memory ~~of claim 55 further~~ comprising:

a chalcogenide memory element having first and second terminals;

a first memory line;

a circuit for selectively precharging said first memory line to either a first or second voltage;

a circuit for supplying a third voltage to the first terminal of said chalcogenide element;

a device for switchably coupling the second terminal of said chalcogenide memory element to said first memory line after said first memory line has been precharged, said device causing a voltage to be applied across said chalcogenide memory element sufficient to write one of two predetermined resistance states in said chalcogenide element depending on which of said first or second voltage is precharged on said memory line; and

at least one capacitor coupled to said memory line to receive and hold said precharge voltage.

Claim 59 (original): The memory cell of claim 58 further comprising a switching device for selectively coupling said at least one capacitor to said memory line.

Claim 60 (currently amended): A ~~The~~ memory ~~of claim 57~~ comprising:

a chalcogenide memory element having first and second terminals;

a first memory line;

a circuit for selectively precharging said first memory line to either a first or second voltage;

a circuit for supplying a third voltage to the first terminal of said chalcogenide element; and

a device for switchably coupling the second terminal of said chalcogenide memory element to said first memory line after said first memory line has been precharged, said device causing a voltage to be applied across said chalcogenide memory element sufficient to write one of two predetermined resistance states in said chalcogenide element depending on which of said first or second voltage is precharged on said memory line;

wherein said memory line has a parasitic capacitance of about 500 fF.

Claim 61 (currently amended): A ~~The~~ memory ~~of claim 55~~ comprising:

a chalcogenide memory element having first and second terminals;

a first memory line;

a circuit for selectively precharging said first memory line to either a first or second voltage;

a circuit for supplying a third voltage to the first terminal of said chalcogenide element; and

a device for switchably coupling the second terminal of said chalcogenide memory element to said first memory line after said first memory line has been precharged, said device causing a voltage to be applied across said chalcogenide memory element sufficient to write one of two predetermined resistance states in said chalcogenide

element depending on which of said first or second voltage is precharged on said memory line;

wherein said chalcogenide memory element comprises a germanium:selenium glass composition which is doped with silver.

Claims 62-64 (cancel):

Claim 65 (currently amended): A ~~The~~ processor system ~~of claim 64~~ comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said precharge circuit supplies a supply voltage as said first voltage to program a higher resistance state into said memory element and ground potential as said first voltage to program a lower resistance state into said memory element, ~~said first value is at or approximately at Vdd, said second value is at or approximately at ground,~~ and said second voltage is at or approximately at one half of said supply voltage. ~~Vdd/2.~~

Claim 66 (cancel):

Claim 67 (currently amended): A ~~The~~ processor system ~~of claim 62~~ comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second

voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 68 (currently amended): A ~~The~~ processor system ~~of claim 62~~ comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claims 69-70 (cancel):

Claim 71 (currently amended): A ~~The~~ processor system ~~of claim 70~~ comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state;

wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.